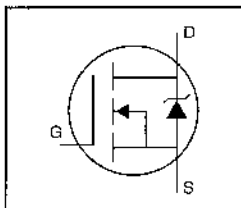


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Isolated Central Mounting Hole
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DS} = 600V$$

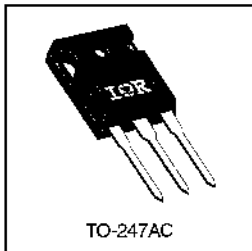
$$R_{DS(on)} = 0.40\Omega$$

$$I_D = 16A$$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.


 DATA
SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	16	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	10	
I_{DM}	Pulsed Drain Current ①	64	
P_D @ $T_C = 25^\circ C$	Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	1000	mJ
I_{AR}	Avalanche Current ①	16	A
E_{AR}	Repetitive Avalanche Energy ①	28	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{DS(BR)}$	600	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{DS(BR)}/\Delta T_J$	—	0.83	—	V/°C	Reference to 25°C , $I_D=1mA$
$R_{DS(on)}$	—	—	0.40	Ω	$V_{GS}=10V, I_D=9.6A$ ②
$V_{GS(th)}$	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
g_{fs}	13	—	—	S	$V_{DS}=50V, I_D=9.6A$ ④
I_{DSS}	—	—	100	μA	$V_{DS}=600V, V_{GS}=0V$
	—	—	500	μA	$V_{DS}=480V, V_{GS}=0V, T_J=125^\circ\text{C}$
I_{GSS}	—	—	100	nA	$V_{GS}=20V$
	—	—	-100	nA	$V_{GS}=-20V$
Q_g	—	—	210	nC	$I_D=16A$
Q_{gs}	—	—	26	nC	$V_{DS}=360V$
Q_{gd}	—	—	110	nC	$V_{GS}=10V$ See Fig. 8 and 13 ④
$t_{d(on)}$	—	19	—	ns	$V_{DS}=300V$
t_r	—	54	—	ns	$I_D=16A$
$t_{d(off)}$	—	110	—	ns	$R_G=4.5\Omega$
t_f	—	56	—	ns	$R_D=18\Omega$ See Figure 10 ④
L_D	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	—	13	—	nH	
C_{iss}	—	3900	—	pF	$V_{GS}=0V$
C_{oss}	—	440	—	pF	$V_{DS}=25V$
C_{rss}	—	98	—	pF	$f=1.0MHz$ See Figure 5



Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	—	—	64	A	
V_{SD}	—	—	1.8	V	$T_J=25^\circ\text{C}, I_S=16A, V_{GS}=0V$ ④
t_{rr}	—	610	920	ns	$T_J=25^\circ\text{C}, I_F=16A$
Q_{rr}	—	6.6	9.9	μC	$di/dt=100A/\mu s$ ④
t_{on}	—	—	—	—	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DS}=50V$, starting $T_J=25^\circ\text{C}$, $L=7.2mH$, $R_G=25\Omega$, $I_{AS}=16A$ (See Figure 12)
- ③ $I_{SD}\leq 16A$, $di/dt\leq 140A/\mu s$, $V_{DS}\leq V_{DS(BR)}$, $T_J\leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

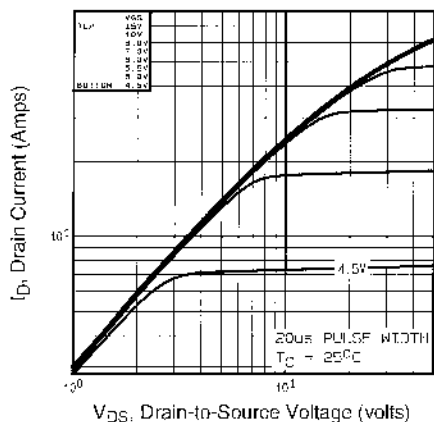


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

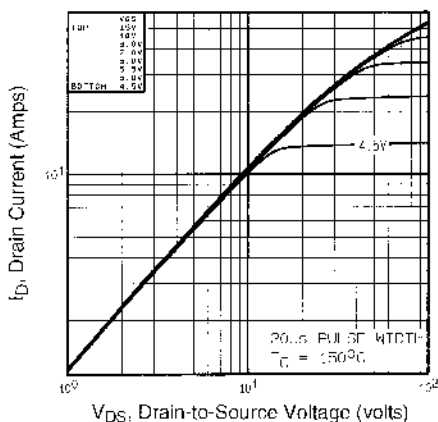


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

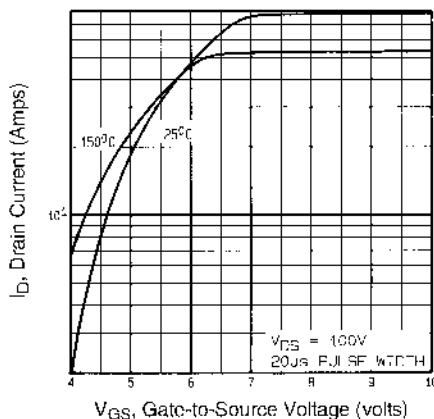


Fig 3. Typical Transfer Characteristics

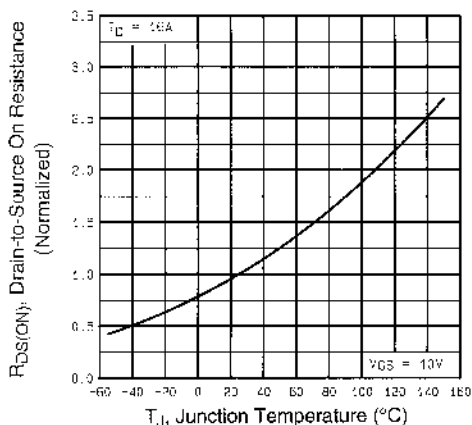


Fig 4. Normalized On-Resistance
Vs. Temperature

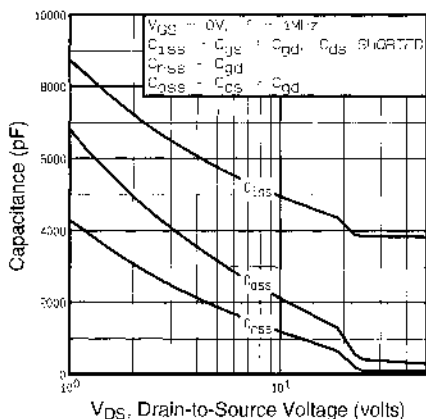


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

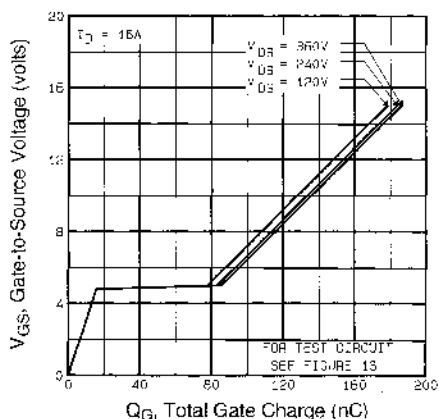


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

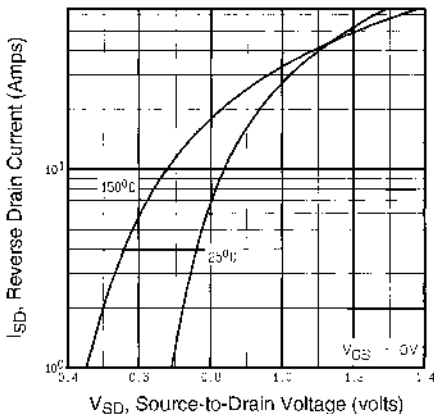


Fig 7. Typical Source-Drain Diode Forward Voltage

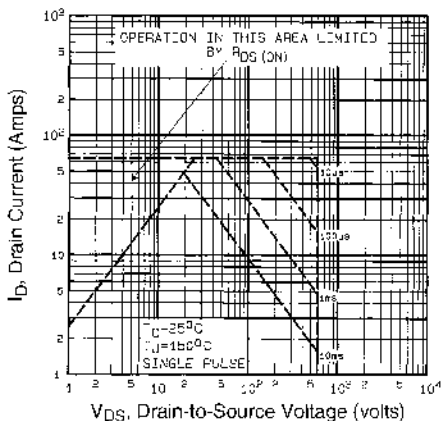


Fig 8. Maximum Safe Operating Area

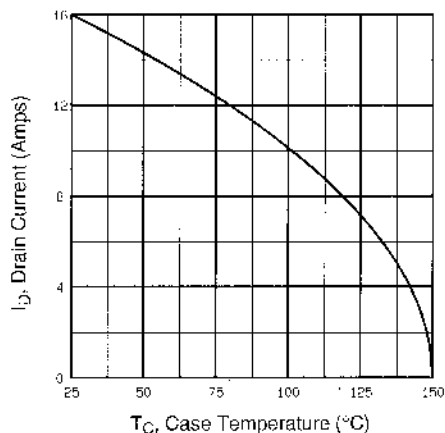


Fig 9. Maximum Drain Current Vs. Case Temperature

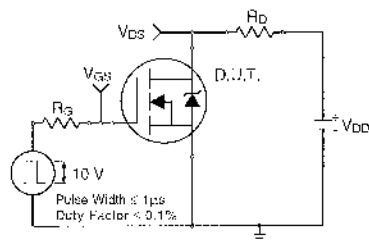


Fig 10a. Switching Time Test Circuit

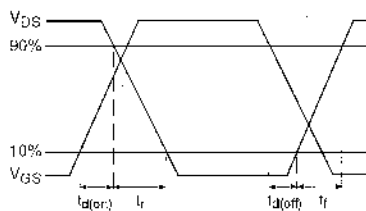


Fig 10b. Switching Time Waveforms

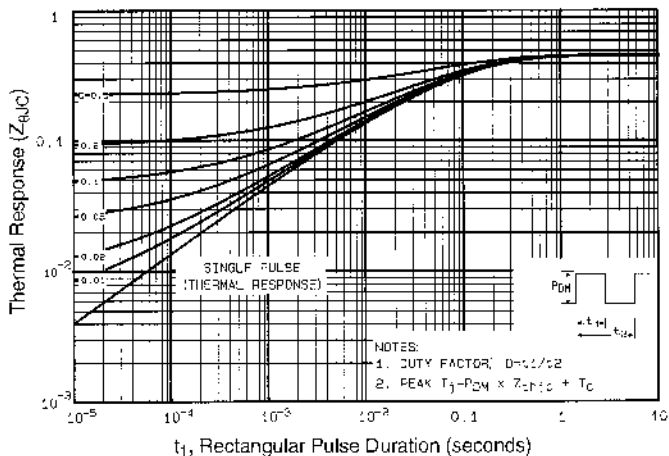


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

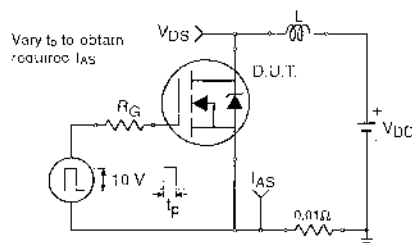


Fig 12a. Unclamped Inductive Test Circuit

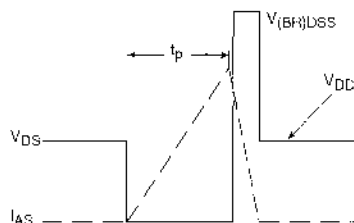


Fig 12b. Unclamped Inductive Waveforms

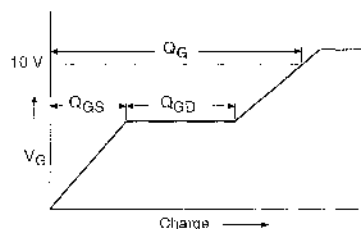


Fig 13a. Basic Gate Charge Waveform

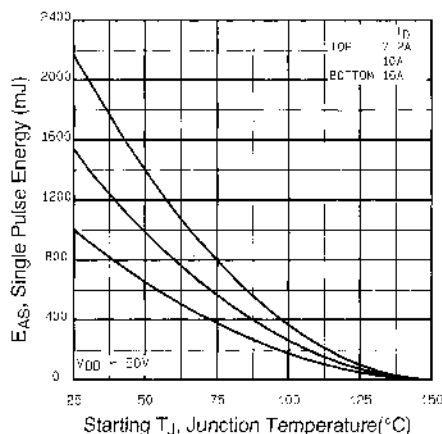


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

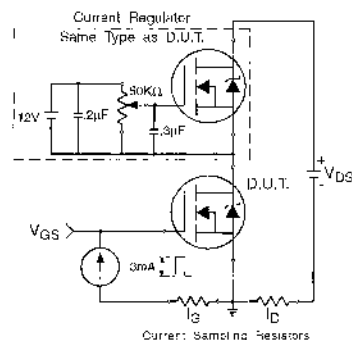


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1511

Appendix C: Part Marking Information – See page 1517

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